

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau



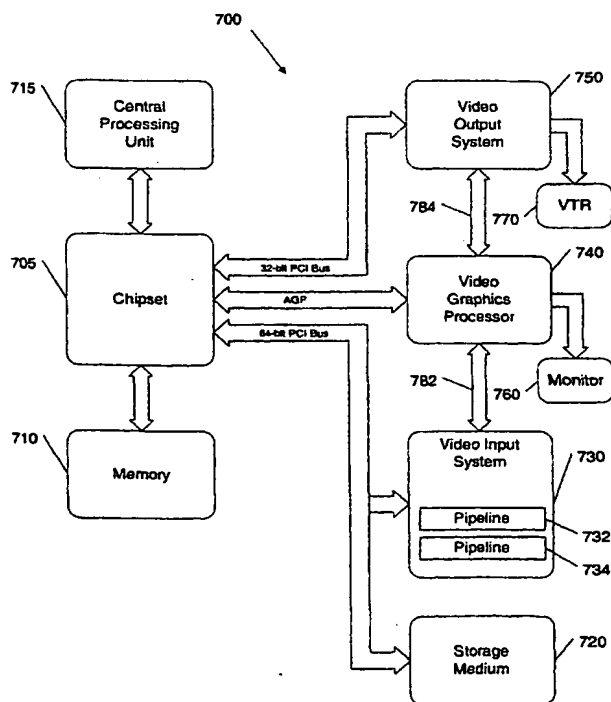
(43) International Publication Date
15 February 2001 (15.02.2001)

PCT

(10) International Publication Number
WO 01/11456 A1

- (51) International Patent Classification⁷: G06F 3/14, H04N 7/26, G06T 1/00
- (21) International Application Number: PCT/US00/21356
- (22) International Filing Date: 4 August 2000 (04.08.2000)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
60/147,609 6 August 1999 (06.08.1999) US
60/147,668 6 August 1999 (06.08.1999) US
- (71) Applicant: INTERGRAPH CORPORATION [US/US];
One Madison Industrial Park, Huntsville, AL 35894-0001 (US).
- (72) Inventors: FORD, Jeff, S.; 122 Progress Lane, Madison, AL 35857 (US). BELOTE, Jeff; 127 Brass Oak Drive, Madison, AL 35758 (US).
- (74) Agents: SUNSTEIN, Bruce, D. et al.; Bromberg & Sunstein LLP, 125 Summer Street, Boston, MA 02110-1618 (US).
- (84) Designated States (*regional*): European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).
- Published:
— With international search report.
- For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: VIDEO CARD WITH INTERCHANGEABLE CONNECTOR MODULE



(57) Abstract: A video card for processing a video signal comprises an interchangeable connector module and a video processing module. The interchangeable connector module has a specific configuration. The video processing module has a connector for coupling the interchangeable connector module. The specific configuration of the video input module sets the characteristics of the video processing module.

BCA A A PU020085
CITED BY APPLICANT

WO 01/11456 A1

VIDEO CARD WITH INTERCHANGEABLE CONNECTOR MODULE

FIELD OF THE INVENTION

5 The invention generally relates to a video graphics workstation and, more particularly, the invention relates to interchangeable connector modules for use in video cards.

BACKGROUND OF THE INVENTION

 In general, a video graphics workstation is a system of hardware and software that allows a user to process a video signal for use in a number of different applications. For example, the user may process a video signal for display on a computer monitor, for storage on a computer-readable storage medium, for display on a television, or for
10 storage on a video tape.

 Typically, however, video graphics workstations are designed to process particular video signals. Thus, most video graphics workstations are not scalable. In other words, most video graphics workstations are not designed to adapt to the changing needs of the workstation's user.

15

SUMMARY OF THE INVENTION

 In accordance with one aspect of the invention, a video input system for processing video signals comprises a video input module and a video processing module. The video input module converts a first live video signal, has a specific configuration, and produces a first formatted video signal. The video processing module pre-processes
20 the first formatted video signal, producing a first pre-processed video signal. The video processing module has a connector for coupling the video input module and the specific configuration of the video input module sets the characteristics of the video processing module.

25 In a further embodiment of the invention, the video input module may further comprises a first receiver for receiving the first live video signal, a processor for

converting the first live video signal into the first formatted video signal, and a buffer for storing the first formatted video signal.

In a still further embodiment of the invention, the video input module may further comprise a second receiver for receiving a second live video signal, a switcher for selecting between the first live video signal and the second live video signal, the switcher forwarding the selected live video signal to the processor for conversion into the first formatted video signal or a second formatted video signal, and the buffer storing the first formatted video signal and the second formatted video signal. The video input module may also include an ancillary data extractor for removing ancillary data from the first live video signal.

In alternate embodiments of the invention, the first live video signal may be an analog composite video signal, an analog component video signal, a serial digital composite video signal, a serial digital component video signal, a parallel digital composite video signal, or a parallel digital component video signal. In addition, the first live video signal may be the same as the second live video signal. Further, the second live video signal may be an analog composite video signal, an analog component video signal, a serial digital composite video signal, a serial digital component video signal, a parallel digital composite video signal, or a parallel digital component video signal. Also, the first formatted video signal may include 20-bits for color data and 10-bits for alpha data. Plus, the first pre-processed video signal may be an RGB encoded video signal, an RGBA encoded video signal, a YUV-Type encoded video signal, or a YUVA-Type encoded video signal.

In further alternate embodiments of the invention, the process of pre-processing may include changing the sample rate of the video signal being pre-processed, gamma removal, gamma insertion, color space conversion, dithering, and scaling. In addition, the process of pre-processing may include addressing on a frame-by-frame basis the video signal being pre-processed. Further, the video input system may be a Peripheral Component Interconnect circuit board.

In still further alternate embodiments of the invention, the pre-processed video signal may be forwarded to a video output system. Or, the pre-processed video signal

may be forwarded to a storage medium. Or, the pre-processed video signal may be forwarded to a video graphics processor.

In accordance with another aspect of the invention, a method and system for producing video signals comprises a video processing module and a video output module. The video processing module post-processes a video signal, producing a post-processed video signal and having a connector for coupling a video output module. The video output module converts the post-processed video signal, has a specific configuration, and produces a formatted video signal. The specific configuration of the video output module sets the characteristics of the video processing module.

In a further embodiment of the invention, the video output module may further comprise a buffer for storing the post-processed video signal, a processor for converting the post-processed video signal into the formatted video signal, and a transmitter for transmitting the formatted video signal.

In a still further embodiment of the invention, the video output module may include an ancillary data injector for inserting ancillary data into the post-processed video signal.

In alternate embodiments of the invention, the video signal may be an RGB encoded video signal, an RGBA encoded video signal, a YUV-Type encoded video signal, or a YUVA-Type encoded video signal. In addition, the formatted video signal may be an analog composite video signal, an analog component video signal, a serial digital composite video signal, a serial digital component video signal, a parallel digital composite video signal, or a parallel digital component video signal.

In further alternate embodiments of the invention, the video signal may be forwarded from a storage medium. Or, the video signal may be forwarded from a video graphics processor. Or, the video signal may be forwarded from a video input system.

In still further alternate embodiments of the invention, the process of post-processing may include region of interest selection, frame rate matching, scaling, picture framing, letter boxing, changing the sample rate of the video signal being post-processed, gamma removal, gamma insertion, color space conversion, and changing frames of video data into interleaved fields of video data. In addition, the process of

post-processing may include addressing on a frame-by-frame basis the video signal being post-processed. Further, the video output system may be a Peripheral Component Interconnect circuit board.

BRIEF DESCRIPTION OF THE DRAWINGS

10 The foregoing and other objects and advantages of the invention will be appreciated more fully from the following further description thereof with reference to the accompanying drawings wherein:

 Figure 1 shows a block diagram of an exemplary video graphics workstation for implementing the various embodiments of the invention.

15 Figures 2a through 2b show various exemplary embodiments for a video input system for use in a video graphics workstation.

 Figure 3 shows an exemplary embodiment for a scalable video input system for use in a video graphics workstation.

20 Figures 4a and 4b show various exemplary exploded views for mounting an interchangeable connector module to a video processing module.

 Figure 5 shows an exemplary embodiment for a video output system for use in a video graphics workstation.

 Figure 6 shows an exemplary embodiment for a scalable video output system for use in a video graphics workstation.

25 Figures 7a through 7g show various exemplary video graphics applications carried out on an exemplary video graphics workstation.

 Figure 8 shows an exemplary process in a video graphics workstation for video signal frame rate matching.

30 Figures 9a and 9b show an exemplary process in a video graphics workstation for packing and unpacking pixels.

DETAILED DESCRIPTION OF THE INVENTION

 In accordance with one embodiment of the invention, a video graphics workstation includes three sub-systems--a video input system, a video graphics

processor, and a video output system. In general, the video input system pre-processes video signals, the video graphics processor processes and/or displays video signals and graphics input, and the video output system produces video signals. The video signals processed and produced may be analog video signals or digital video signals.

Figure 1 shows a block diagram of an exemplary video graphics workstation for implementing the various embodiments of the invention. Video graphics workstation 100 includes central processing unit 102, chipset 104, memory 106, two Peripheral Component Interconnect ("PCI") buses--a 64-bit PCI bus and a 32-bit PCI bus, and an Accelerated Graphics Port ("AGP"). Video input system 110 and storage medium 120 connect to chipset 104 via the 64-bit PCI bus. Video graphics processor 130 connects to chipset 104 via the AGP. Video output system 140 connects to chipset 104 via the 32-bit PCI bus. In addition, video input system 110 connects to video graphics processor 130 via local bus 182 and video output system 140 connects to video graphics processor 130 via local bus 184.

A. Video Input System

Figures 2a through 2b show various exemplary embodiments for video input system 110. In particular, Figure 2a shows an exemplary embodiment for pre-processing a live video signal in video input system 110. The process of pre-processing a video signal includes, among other things, up sampling, down sampling, gamma insertion, gamma removal, color space conversion, scaling and dithering. For purposes of understanding and reference, and without intending to limit the meaning the above-identified processes have to a person of ordinary skill in the art, listed below are definitions for the above-identified processes:

PROCESS	DEFINITION
Up Sampling	Process of increasing the amount of digital data used to represent an image
Down Sampling	Process of decreasing the amount of digital data used to represent an image

PROCESS	DEFINITION
Gamma Insertion	Process of inserting a value to compensate for the non-linear characteristics of an output device (e.g., a computer monitor)
Gamma Removal	Process of removing a value inserted to compensate for the non-linear characteristics of an output device (e.g., a computer monitor)
Color Space Conversion	Process of converting between different color encoding schemes (e.g., between a component color scheme and a composite color scheme)
Scaling	Process of changing the resolution of an image
Dithering	Process of combining colors to trick the eye into seeing more colors than the system can actually display

In addition, pre-processing may include addressing on a frame-by-frame basis the video signal being pre-processed. In video, a frame is a single complete image. In frame-by-frame addressing, video input system 110 may pre-process one frame of a video signal different than, for example, the next frame of the video signal.

In the embodiment shown in Figure 2a, video input system 110 includes video input module 200, input multiplexer 212, input multiplexer 222, pipeline 210, pipeline 220, output multiplexer 214, and output multiplexer 224. Video input module 200 receives a live video signal and forwards the live video signal to, for example, a buffer (not shown) for transfer to pipeline 210 and/or pipeline 220. The live video signal may be an analog video signal or a digital video signal. If the live video signal is an analog video signal, then video input module 200 converts the live video signal into a computer-readable format.

The input multiplexers, multiplexer 212 and multiplexer 222, route the respective video signal to the pipelines. In particular, multiplexer 212 routes video signals to pipeline 210 and multiplexer 222 routes video signals to pipeline 220. The pipelines,

pipeline 210 and pipeline 220, pre-process the forwarded video signal. The output multiplexers, multiplexer 214 and multiplexer 224, route the pre-processed video signals to, for example, various output buffers (not shown) accessible to video graphics workstation 100. For example, the pre-processed video signal may be forwarded, via the 64-bit PCI bus and the AGP, to video graphics processor 130. Or, the pre-processed video signal may be forwarded, via the 64-bit PCI bus and the 32-bit PCI bus, to video output system 140. The pre-processed video signal may also be forwarded, via the 64-bit bus, to storage medium 120.

Figure 2b shows an exemplary embodiment for pre-processing a live video signal and a stored video signal in video input system 110. In this embodiment, pipeline 210 and pipeline 220 pre-process a live video signal and/or a stored video signal. Typically, the stored video signal is forwarded from, for example, storage medium 120, to a buffer (not shown) to allow for efficient transfer of the stored video signal to video input system 110.

With two pipelines, a single live, or stored, video signal may reach pipeline 210 and pipeline 220. Thus, two versions of a single live, or stored, video signal may be generated at the same time. For example, video input system 110 may receive a television signal and pre-process the television signal via pipeline 210 for display on a computer monitor and via pipeline 220 for storage on storage medium 120. In addition, using frame-by-frame addressing, video input system 110 may pre-process more than two video signals substantially at the same time. In this embodiment, the frames of the different video signals are interleaved and routed to pipeline 210 and pipeline 220. Moreover, video input system 110 may pass a video signal, either live or stored, through pipeline 210 and/or pipeline 220 without pre-processing the video signal.

In a further embodiment of video input system 110, video input module 200 receives and forwards more than one live video signal to, for example, a buffer (not shown) for transfer to pipeline 210 and/or pipeline 220. The live video signals may be analog video signals or digital video signals. If the live video signal is an analog video signal, then video input module 200 converts the live video signal into a computer-

readable format. For each received live video signal, video input module 200 produces a forwarded video signal.

In a further embodiment of these exemplary embodiments, video input module 200 includes an ancillary data extractor for removing ancillary data from a live video signal. Typically, the ancillary data is removed from the live video signal prior to receipt
10 of the live video signal in the input multiplexers, multiplexer 212 and multiplexer 214. Ancillary data includes, among other things, audio data and close captioning data.

Figure 3 shows an exemplary embodiment for a scalable video input system 110. In this embodiment, video input system 110 includes video input module 300 and video processing module 350. Video input module 300 includes receiver 302, processor 304,
15 and buffer 306. Receiver 302 receives a live video signal and forwards the live video signal to processor 304. Processor 304 converts the received video signal into a video signal having a common video data format. The formatted video signal is then forwarded to buffer 306 for transfer to video processing module 350. In alternate embodiments of the invention, video input module 300 may include an ancillary data
20 extractor for removing ancillary data from a live video signal.

Video processing module 350 includes input multiplexer 352, pipeline 354, and output multiplexer 356. As discussed above in regard to the embodiments shown in Figure 2, video processing module 350 pre-processes the formatted video signal and/or a stored video signal and routes the pre-processed video signal to, for example, a buffer
25 (not shown) accessible to video graphics workstation 100. Video processing module 350 may have two pre-processing pipelines. In addition, the pre-processed video signal may be forwarded to video graphics processor 130, video output system 140, and/or storage medium 120.

The common video data format may be an organized bit stream. As noted above,
30 a frame is a single complete image. An image, in turn, is composed of a raster of picture elements, referred to as pixels. A pixel is represented by some number of bits stored, for example, in memory. Pixels are the smallest "units" on a screen that can be given a color (represented with color data) and an opacity (represented with alpha data). Thus, an organized bit stream may include color data, alpha data, or color data and alpha data.

For example, a bit stream with color data may include 20-bits for color data. In contrast, a bit stream for alpha data may include 10-bits for alpha data. Pipeline 354 may pre-process color data separate from alpha data. In this embodiment, a color data bit stream may be forwarded on a output different from the output used to forward alpha data.

10 In these exemplary embodiments, video input module 300 and video processing module 350 are separate modules coupled together via, for example, male/female cables. In one embodiment, video input module 300 is a daughterboard that plugs into video processing module 350. The separation of the various functions of a video input system into a video input module and a video processing module allows for the separation of video input module 300 and video processing module 350.

15 In turn, the separation of video input module 300 from video processing module 350 allows for the configuration of various video input modules, each configured to receive and process different video signal formats. Because the “input” functions of video input system 110 have been separated from the “processing” functions of video input system 110, video input module 300 may be “exchanged” without the need to
20 replace video processing module 350. Thus, when a user wants to input, for example, a serial digital component video signal into video input system 110 instead of an analog composite video signal, the user “exchanges” the video input module configured for the analog composite video signal with a video input module configured for the serial digital component video signal. In turn, processor 304 (on the “new” video input module)
25 signals video processing module 350 of the new configuration.

30 Figures 4a and 4b show various exemplary exploded views for mounting an interchangeable connector module, such as video input module 300, to a processing module, such as video processing module 350. In Figure 4a, interchangeable connector module 400 includes connectors 402 and mounting holes 404. Circuit board 450 includes plate 455. Plate 455 includes connector holes 452 and mounting holes 454. Plate assembly 430 includes plate 435a and two screws (not shown). Plate 435a includes connector holes 432a and mounting holes 434a. Connectors 402 are designed to fit through connector holes 432 and 452. The two screws, passing through mounting holes

434a and mounting holes 454, secure interchangeable connector module 400 to circuit board 450 via mounting holes 404.

In Figure 4b, plate assembly 430 further includes plate 435b and gaskets 436. Gaskets 436 are designed to improve electromagnetic shielding. For example, gaskets 436 may be composed of a rubber compound with embedded silver. For the exemplary
10 embodiments shown in both Figure 4a and Figure 4b, in operation, interchangeable connector module 400 would also be coupled (not shown) to processing module 450.

B. Video Graphics Processor

Various exemplary embodiments of a video graphics processor are disclosed in the following:

15 1. U.S. Patent Application Serial No. 09/353,495, filed July 15, 1999, and entitled "MULTIPROCESSOR GRAPHICS ACCELERATOR," the disclosure of which is hereby incorporated, in its entirety, by reference;

20 2. U.S. Patent Application Serial No. 09/354,462, filed July 15, 1999, and entitled "APPARATUS AND METHOD OF DIRECTING GRAPHICAL DATA TO A DISPLAY DEVICE," the disclosure of which is hereby incorporated, in its entirety, by reference;

25 3. U.S. Patent Application Serial No. 09/353,420, filed July 15, 1999, and entitled "WIDE INSTRUCTION WORD GRAPHICS PROCESSOR," the disclosure of which is hereby incorporated, in its entirety, by reference; and

30 4. U.S. Patent Application Serial No. 09/353,419, filed July 15, 1999, and entitled "SYSTEM FOR DISPLAYING A TELEVISION SIGNAL ON A COMPUTER MONITOR," the disclosure of which is hereby incorporated, in its entirety, by reference.

C. Video Output System

Figure 5 shows an exemplary embodiment for video output system 140. In
30 Figure 5, video output system 140 includes receiver 500, pipeline 510, and video output module 520. Receiver 500 receives a video signal and forwards the received video signal to, for example, a buffer (not shown) for transfer to pipeline 510. The received video signal may be formatted in one of many different video data formats. For example, the received video signal may be an RGB encoded video signal or an RGBA

encoded video signal. An RGB encoded video signal encodes an image in accordance with the amount of red, green, or blue contained in the image. An RGBA encoded video signal further encodes an image in accordance with the amount of opacity contained in the image.

The received video signal may also be a "YUV-Type" encoded video signal or a "YUVA-Type" encoded video signal. A "YUV-Type" encoded video signal encodes an image in accordance with the amount of luma (black and white) and color differences contained in the image. A "YUVA-Type" encoded video signal further encodes an image in accordance with the amount of opacity contained in the image. A "YUV-Type" encoded video signal includes, among other things, a YUV encoded video signal, a YCbCr encoded video signal, and a YPbPr encoded video signal. A "YUVA-Type" encoded video signal includes, among other things, a YUVA encoded video signal, a YCbCrA encoded video signal, and a YPbPrA encoded video signal.

Pipeline 510 post-processes the forwarded video signal and forwards the post-processed video signal to video output module 520. The process of post-processing includes, among other things, region of interest selection, frame rate matching, spatial adaptation, up sampling, down sampling, gamma insertion, gamma removal, and color space conversion. Spatial adaptation includes, among other things, scaling and picture framing. Picture framing includes, among other things, letter boxing. For purposes of understanding and reference, and without intending to limit the meaning the above-identified processes have to a person of ordinary skill in the art, listed below are definitions for the above-identified processes not previously defined:

PROCESS	DEFINITION
Region of Interest Selection	Process of selecting a portion of an image for post-processing
Frame Rate Matching	<u>See</u> Section E.
Picture Framing and Letter Boxing	Process of positioning an image on a background image

In addition, post-processing may include addressing on a frame-by-frame basis the video signal being post-processed. In frame-by-frame addressing, video output system 140 may post-process one frame of a video signal different than, for example, the next frame of the video signal. Also, post-processing may include changing a frame of video data into interlaced fields of video data. In using this process, video output system 140 “blends” single or multiple lines from a frame in an input video signal into a single line in an output video signal, e.g., 3:2 pull-down.

Video output module 520 converts the post-processed video signal to a formatted video signal. The formatted video signal may be an analog video signal or a digital video signal.

Typically, video output system 140 also includes a generator locking device, referred to as a genlock, which allows the synchronized display of graphics and video. A genlock may lock video output system 140 to, for example, video graphics processor 130. In addition, regardless of whether video output system 140 is locked to video graphics processor 130, a genlock may lock video output module 520 to another source, e.g., an external clock, an internal clock, etc.

In a further embodiment of these exemplary embodiments, video output module 520 includes an ancillary data injector for inserting ancillary data into the post-processed video signal prior to conversion of the post-processed video signal. As noted above, ancillary data includes, among other things, audio data and close captioning data.

Figure 6 shows an exemplary embodiment for a scalable video output system 140. In this embodiment, video output system 140 includes video processing module 600 and video output module 650. Video processing module 600 includes receiver 602 and pipeline 604. As discussed above in regard to the embodiments shown in Figure 3, video processing module 600 receives a video signal, post-processes the received video signal, and forwards the post-processed video signal to video output module 650. Video processing module 600 may include a generator locking device for locking video processing module 600 to, for example, video graphics processor 130.

Video output module 650 includes buffer 652, processor 654, and transmitter 656. Video processing module 600 forwards the post-processed video signal to buffer

652 for transfer to processor 654. Processor 654 converts the post-processed video signal into a formatted video signal, e.g., an analog composite video signal, a parallel digital component video signal, etc. The formatted video signal is then forwarded to transmitter 656. In alternate embodiments of the invention, video output module 650 may include an ancillary data injector for inserting ancillary data into the post-processed video signal.

In these exemplary embodiments, video output module 650 and video processing module 600 are separate modules coupled together via, for example, male/female cables. In one embodiment, video output module 650 is a daughterboard that plugs into video processing module 600. The separation of the various functions of a video output system into a video output module and a video processing module allows for the separation of video output module 650 and video processing module 600.

In turn, the separation of video output module 650 from video processing module 600 allows for the configuration of various video output modules, each configured to process and produce different video signal formats. Because the “output” functions of video output system 140 have been separated from the “processing” functions of video output system 140, video output module 650 may be “exchanged” without the need to replace video processing module 600. Thus, when a user wants to output, for example, a serial digital component video signal instead of an analog composite video signal, the user “exchanges” the video output module configured for the analog composite video signal with a video output module configured for the serial digital component video signal. In turn, processor 354 (on the “new” video output module) signals video processing module 600 of the new configuration.

As an interchangeable connector module, video output module 650 may be mounted on video processing module 600, a processing module, in the manner shown in Figures 4a and 4b.

D. Exemplary Video Graphics Applications

Figures 7a through 7g show various exemplary video graphics applications carried out on an exemplary video graphics workstation implementing one embodiment of the invention. In this embodiment, video input system 730 includes two pipelines,

pipeline 732 and pipeline 734. In addition, video output system 750 forwards a formatted video signal to a video tape recorder for recordation.

In Figure 7a, video graphics workstation 700 captures a live video signal. First, video graphics workstation 700 receives the live video signal. Next, the received video signal is pre-processed in pipeline 732 of video input system 730. Then, the pre-processed video signal is forwarded, via the 64-bit PCI bus, to storage medium 720.

In Figure 7b, video graphics workstation 700 captures and displays a live video signal. First, video graphics workstation 700 receives the live video signal. Next, the received video signal is pre-processed in both pipeline 732 and pipeline 734 of video input system 730. Then, the pre-processed video signal from pipeline 732 is forwarded, via the 64-bit PCI bus, to storage medium 720. In the interim, the pre-processed video signal from pipeline 734 is forwarded, via local bus 782, to video graphics processor 740 for display on computer monitor 760. The pre-processed video signal from pipeline 734 may also be forwarded to video graphic processor 740 via the 64-bit PCI bus and the AGP. In alternate embodiment, the pre-processed video signal from pipeline 734 may be forwarded, via the 64-bit bus and the 32-bit bus, to video output system 750 for recordation on video tape recorder 770.

In Figure 7c, video graphics workstation 700 plays back a stored video signal. First, video graphics workstation 700 forwards a stored video signal, via the 64-bit PCI bus to video input system 730. Next, the stored video signal is pre-processed in pipeline 732. Then, the pre-processed video signal is forwarded, via local bus 782, to video graphics processor 740 for display on computer monitor 760. In an alternate embodiment, the pre-processed video signal may also forwarded, via local bus 784, to video output system 750 for recordation on video tape recorder 770.

In Figure 7d, video graphics workstation 700 processes a stored video signal, for example, performs a two-dimensional or three-dimensional effect on the stored video signal, and displays the processed video signal. First, video graphics workstation 700 forwards a stored video signal, via the 64-bit PCI bus, to video input system 730. Next, the stored video signal is pre-processed in pipeline 732. Then, the pre-processed video signal is forwarded, via local bus 782, to video graphics processor 740 for "effects"

processing and display on computer monitor 760. In an alternate embodiment, the processed video signal may also be forwarded, via local bus 784, to video output system 750 for recordation on video tape recorder 770.

10 In Figure 7e, video graphics workstation 700 pre-processes a stored video signal and saves the pre-processed video signal. First, video graphics workstation 700 forwards a stored video signal, via the 64-bit PCI bus, to video input system 730. Next, the stored video signal is pre-processed in pipeline 732. Then, the pre-processed video signal is forwarded, via the 64-bit PCI bus, to storage medium 720. In alternate embodiments, the pre-processed video signal may be forwarded, via the 64-bit PCI bus, to central processing unit 715 or to memory 710.

15 In Figure 7f, video graphics workstation 700 processes a stored video signal and saves the processed video signal. First, video graphics workstation 700 forwards a stored video signal, via the 64-bit PCI bus, to video input system 730. Next, the stored video signal is pre-processed in pipeline 732. Then, the pre-processed video signal is forwarded, via local bus 782, to video graphics processor 740 for "effects" processing. 20 Last, the processed video signal is forwarded, via local bus 782, to video input system 730. Video input system 730 may pre-process the processed video signal, for example, to convert the processed signal to a format better suited for saving, or forward the processed signal, via the 64-bit PCI bus, to storage medium 720.

25 In Figure 7g, video graphics workstation 700 combines a live video signal, a stored video signal, and graphics information and records the combined video signal. First, video graphics workstation 700 receives a live video signal. Next, the received video signal is pre-processed in pipeline 732 of video input system 730. In the interim, video graphics workstation 700 forwards a stored video signal to video input system 730. Next, the stored video signal is pre-processed in pipeline 734. Then, graphics 30 information (via the AGP), the pre-processed video signal from pipeline 732 (via local bus 782), and the pre-processed video signal from pipeline 734 (via local bus 782) are forwarded to video graphics processor 740 for "effects" processing. Last, the processed video signal is forwarded, via local bus 784, to video output system 750 for recordation on video tape recorder 770.

E. Frame Rate Matching

As discussed above, a frame is a single complete image. Typically, a frame is represented, in a video graphics workstation, with frame data. In general, frame rate is how fast a new frame of frame data, in other words, an new image, is available for processing or display. The process of frame rate matching includes, among other things, matching the frame rate of, for example, a video signal to the frame rate of, for example, an output device. Typically, in a video graphics workstation, the process of frame rate matching occurs in the video output system.

Figure 8 shows an exemplary process in a video graphics workstation for video signal frame rate matching. The process begins at step 800, in which the video graphics workstation fills a first buffer with a sequence of frame data. Next, at step 810, the workstation reads out the frame data in the first buffer and, at substantially the same time, fills a second buffer with the next sequence of frame data. The process continues at step 820, in which the video graphics workstation determines whether all of the frame data has been read out of the first buffer. If yes, the video graphics workstation fills the first buffer with the next sequence of frame data. If no, the video graphics workstation, at step 830, fills the third buffer with the next sequence of frame data.

Next, at step 840, the video graphics workstation determines whether all of the frame data in the first buffer has been read out of the first buffer. If no, the video graphics workstation begins to fill the second buffer with the next sequence of frame data. If yes, the video graphics workstation, at step 850, determines whether the second buffer or the third buffer has the most current and most complete frame data. If the second buffer has the most current and most complete frame data, the video graphics workstation, at step 860, reads the frame data out of the second buffer. If the third buffer has the most current and most complete frame data, the video graphics workstation, at step 870, reads the frame data out of the third buffer.

In a further embodiment of the invention, the buffer determined not to have been filled with the most current and most complete frame data becomes a remainder buffer. In this embodiment, the video graphics workstation fills the remainder buffer with the next sequence of frame data. Then, if all of the frame data has not been read out of the

buffer determined to have been filled with the most current and most complete frame data, the video graphics workstation fills the first buffer with the next sequence of frame data. The video graphics workstation continues to alternate between the remainder buffer and the first buffer until all of the frame data has been read out of the buffer determined to have been filled with the most current and most complete frame data.

10 Thus, in operation, the three buffers change "roles." For example, the buffer now being filled may, depending upon the circumstances, next become either the buffer being read or the buffer not being either filled or read. Or, the buffer now being read may, depending upon the circumstances, next become either the buffer being filled or the buffer not being either filled or read. Or, the buffer now not being either filled or read
15 may, depending upon the circumstances, next become either the buffer being read or the buffer being filled.

 In both embodiments of the invention, a buffer may contain the most complete frame data when the buffer is less than 100% full. Typically, however, a buffer contains the most complete frame data when the buffer is 100% full. In addition, a buffer may
20 contain one or more frames of frame data. Typically, however, a buffer contains one frame of frame data.

 Further, both embodiments of the invention are scalable. In other words, both embodiments of the invention may be used to match any frame rates. For example, a frame rate to be matched may be 24/1.001 frames/second, or 24 frames/second, or 25
25 frames/second, or 29.97 frames/second, or 30/1.001 frames/second, or 30 frames/second, or 50 frames/second, 60/1.001 frames/second, 60 frames/second or 75 frames/second. Also, the frame rates being matched may be the same frame rate. Or, in the alternative, the frame rates being matched may be multiples of each other.

F. Packing and Unpacking Video Data

30 As discussed above, an image is composed of a raster of picture elements, referred to as pixels. Pixels are the smallest "units" on a screen that can be given a color (represented with color data) and an opacity (represented with alpha data). In general, a pixel is represented by some number of bits stored, for example, in memory. For

example, a pixel may be 1-bit in length, 8-bits in length, 10-bits in length, 24-bits in length, or 32-bits in length.

In turn, memory stores data in segments, with each segment being some number of bits. For example, memory may be capable of storing data in 32-bit segments or 64-bit segments. It may be inefficient, however, to store, for example, one 8-bit pixel in a 32-bit memory segment. But, four 8-bit pixels may be "packed" in a 32-bit memory segment. In the same way, four 24-bit pixels may be packed in three 32-bit memory segments. Typically, in a video graphics workstation, the process of packing and unpacking pixels occurs in the video input system.

Figures 9a and 9b show an exemplary process in a video graphics workstation for packing and unpacking pixels. In particular, Figure 9a shows an exemplary process in a video graphics workstation for unpacking pixels. The process begins at step 900a, in which the video graphics workstation loads a shift-down register with the pixel data contained in a first memory device. In this embodiment, the first memory device has a bit storage capacity smaller in size than the bit storage capacity of the shift-down register. For example, the first memory device may be 64-bits in length and the shift-down register may be 80-bits in length. Next, at step 910a, the video graphics workstation shifts one complete pixel of pixel data down the shift-down register. For example, one 24-bit pixel is shifted down the shift-down register.

Then, at step 920a, the video graphics workstation determines whether the shift-down register contains another complete pixel of pixel data. If yes, the video graphics workstation shifts another complete pixel of pixel data down the shift-down register. If no, the video graphics workstation, at step 930a, loads a shift-up register with the pixel data contained in a second memory device. In this embodiment, the second memory device is contiguous with the first memory device and has the same bit storage capacity as the first memory device. Also, the shift-up register has the same bit storage capacity as the shift-down register.

Next, at step 940a, the video graphics workstation shifts the pixel data in the shift-up register up the number of bits of pixel data remaining in the shift-down register. For example, if the shift-down register has 16 bits of pixel data remaining, then the video

graphics workstation shifts the pixel data in the shift-up register up 16 bits. Then, at step 950a, the video graphics workstation moves the pixel data in the shift-up register to the shift-down register, placing the shifted-up pixel data in the same bit locations in the shift-down register the shifted-up pixel data occupied in the shift-up register. For example, if the shifted-up pixel data occupied bit locations 16 through 63 in the shift-up register, then the video graphics workstation moves the shifted-up pixel data to bit locations 16 through 63 in the shift-down register.

Figure 9b shows an exemplary process in a video graphics workstation for packing pixels. In this embodiment, the memory device in which the pixel data will be packed has a bit storage capacity smaller in size than the bit storage capacity of the shift-up register. For example, the memory device may be 64-bits in length and the shift-up register may be 80-bits in length.

The process begins at step 900b, in which the video graphics workstation shifts one complete pixel of data up a shift-up register. Next, at step 910b, the video graphics workstation determines whether the shift-up register has capacity to hold another complete pixel of pixel data. If yes, the video graphics workstation shifts another complete pixel of pixel data up the shift-up register. If no, the video graphics workstation, at step 920b, moves the pixel data in the uppermost bit locations of the shift-up register to a shift-down register, placing the moved pixel data in the same bit locations in the shift-down register the moved pixel data occupied in the shift-up register. For example, if the moved pixel data occupied bit locations 16 through 63 in the shift-up register, then the video graphics workstation moves the shifted-up pixel data to bit locations 16 through 63 in the shift-down register.

The amount of pixel data moved from the uppermost bit locations in the shift-up register depends upon the bit storage capacity of the memory device in which the pixel data will be packed. For example, if the memory device is 64-bits in length, then the video graphics workstation moves the 64 uppermost bits of the shift-up register to the shift-down register. Also, the shift-down register has the same bit storage capacity as the shift-up register.

Next, at step 930b, the video graphics workstation shifts the pixel data in the shift-down register down the number of bits of pixel data remaining in the shift-up register. For example, if the shift-up register has 16 bits of pixel data remaining, then the video graphics workstation shifts the pixel data in the shift-down register down 16 bits. Then, at step 940b, the video graphics workstation moves the contents of the shift-down register to the memory device.

In all embodiments of the invention, one complete pixel of pixel data may include a bit stream of color data, a bit stream of alpha data, or a bit stream of color data and alpha data. The color data may be RGB encoded or "YUV-Type" encoded. In addition, the color data and alpha data may be RGBA encoded or "YUVA-Type" encoded.

The various embodiments of the invention may be implemented in any conventional computer programming language. For example, the various embodiments may be implemented in a procedural programming language (for example, "C") or an object-oriented programming language (for example, "C++" or JAVA). The various embodiments of the invention may also be implemented as preprogrammed hardware elements (for example, application specific integrated circuits or digital processors), or other related components.

The various embodiments of the invention may be also implemented as a computer program product for use with a computer system. Such implementation may include a series of computer instructions fixed either on a tangible medium, such as a computer readable media (for example, a diskette, CD-ROM, ROM, or fixed disk), or transmittable to a computer system via a modem or other interface device, such as a communications adapter connected to a network over a medium. The medium may be either a tangible medium (for example, optical or analog communications lines) or a medium implemented with wireless techniques (for example, microwave, infrared or other transmission techniques). The series of computer instructions preferably embodies all or part of the functionality previously described herein with respect to the system. Those skilled in the art should appreciate that such computer instructions can be written in a number of programming languages for use with many computer architectures or

operating systems. Furthermore, such instructions may be stored in any memory device, such as semiconductor, magnetic, optical or other memory devices, and may be transmitted using any communications technology, such as optical, infrared, microwave, or other transmission technologies. It is expected that such a computer program product may be distributed as a removable medium with accompanying printed or electronic documentation (for example, shrink wrapped software), pre-loaded with a computer system (for example, on system ROM or fixed disk), or distributed from a server or electronic bulletin board over the network (for example, the Internet or World Wide Web).

Although various exemplary embodiments of the invention have been disclosed, it should be apparent to those skilled in the art that various changes and modifications can be made which will achieve some of the advantages of the invention without departing from the true scope of the invention. These and other obvious modifications are intended to be covered by the appended claims.

We claim:

1. A video input system for processing video signals, the system comprising:
a video input module for converting a first live video signal, the video input module having a specific configuration and producing a first formatted video signal; and
10 a video processing module for pre-processing the first formatted video signal, the video processing module producing a first pre-processed video signal, the video processing module having a connector for coupling the video input module, the specific configuration of the video input module setting the characteristics of the video processing module.
15
2. The video input system according to claim 1, the video input module further comprising:
a first receiver for receiving the first live video signal;
a processor for converting the first live video signal into the first formatted video
20 signal; and
a buffer for storing the first formatted video signal.
3. The video input system according to claim 2, the video input module further comprising:
25 a second receiver for receiving a second live video signal;
a switcher for selecting between the first live video signal and the second live video signal, the switcher forwarding the selected live video signal to the processor for conversion into the first formatted video signal or a second formatted video signal; and
the buffer storing the first formatted video signal and the second formatted video
30 signal.
4. The video input system according to claim 1 wherein the video input module includes an ancillary data extractor for removing ancillary data from the first live video signal.

5. The video input system according to claim 1 wherein the first live video signal is VS, wherein VS is an analog composite video signal, an analog component video signal, a serial digital composite video signal, a serial digital component video signal, a parallel digital composite video signal, or a parallel digital component video signal.

10 6. The video input system according to claim 3 wherein the first live video signal is the same as the second live video signal.

15 7. The video input system according to claim 3 wherein the first live video signal is first-VS, wherein first-VS is a first analog composite video signal, a first analog component video signal, a first serial digital composite video signal, a first serial digital component video signal, a first parallel digital composite video signal, or a first parallel digital component video signal and the second live video signal is second-VS, wherein second-VS is a second analog composite video signal, a second analog component video signal, a second serial digital composite video signal, a second serial digital component video signal, a second parallel digital composite video signal, or a second parallel digital component video signal.

20 8. The video input system according to claim 1 wherein the first formatted video signal includes 20-bits for color data and 10-bits for alpha data.

25 9. The video input system according to claim 1 wherein the first pre-processed video signal is e-VS, wherein e-VS is an RGB encoded video signal, an RGBA encoded video signal, a YUV-Type encoded video signal, or a YUVA-Type encoded video signal.

30 10. The video input system according to claim 1 wherein the process of pre-processing includes changing the sample rate of the video signal being pre-processed.

11. The video input system according to claim 1 wherein the process of pre-processing includes gamma removal.

12. The video input system according to claim 1 wherein the process of pre-processing includes gamma insertion.

13. The video input system according to claim 1 wherein the process of pre-processing includes color space conversion.

14. The video input system according to claim 1 wherein the process of pre-processing includes dithering.

15. The video input system according to claim 1 wherein the process of pre-processing includes scaling.

16. The video input system according to claim 1 wherein the process of pre-processing includes addressing on a frame-by-frame basis the video signal being pre-processed.

17. The video input system according to claim 1 wherein the pre-processed video signal is forwarded to a video output system.

18. The video input system according to claim 1 wherein the pre-processed video signal is forwarded to a storage medium.

19. The video input system according to claim 1 wherein the pre-processed video signal is forwarded to a video graphics processor.

20. The video input system according to claim 1 wherein the system is a Peripheral Component Interconnect circuit board.

21. A video output system for producing video signals, the system comprising:

a video processing module for post-processing a video signal, the video processing module producing a post-processed video signal and having a connector for coupling a video output module; and

a video output module for converting the post-processed video signal, the video output module having a specific configuration and producing a formatted video signal, the specific configuration of the video output module setting the characteristics of the video processing module.

22. The video output system according to claim 21, the video output module further comprising:

a buffer for storing the post-processed video signal;
a processor for converting the post-processed video signal into the formatted video signal; and
a transmitter for transmitting the formatted video signal.

23. The video output system according to claim 21 wherein the video output module includes an ancillary data injector for inserting ancillary data into the post-processed video signal.

24. The video output system according to claim 21 wherein the video signal is e-VS, wherein e-VS is an RGB encoded video signal, an RGBA encoded video signal, a YUV-Type encoded video signal, or a YUVA-Type encoded video signal.

25. The video output system according to claim 21 wherein the video signal is forwarded from a storage medium.

26. The video output system according to claim 21 wherein the video signal is forwarded from a video graphics processor.

27. The video output system according to claim 21 wherein the video signal is forwarded from a video input system.

28. The video output system according to claim 21 wherein the formatted video signal is VS, wherein VS is an analog composite video signal, an analog component video signal, a serial digital composite video signal, a serial digital component video signal, a parallel digital composite video signal, or a parallel digital component video signal.

29. The video output system according to claim 21 wherein the process of post-processing includes region of interest selection.

30. The video output system according to claim 21 wherein the process of post-processing includes frame rate matching.

31. The video output system according to claim 21 wherein the process of post-processing includes spatial adaptation.

32. The video output system according to claim 31 wherein the process of spatial adaptation includes scaling.

33. The video output system according to claim 31 wherein the process of spatial adaptation includes picture framing.

34. The video output system according to claim 33 wherein the process of picture framing includes letter boxing.

35. The video output system according to claim 21 wherein the process of post-processing includes changing the sample rate of the video signal being post-processed.

36. The video output system according to claim 21 wherein the process of post-processing includes gamma removal.

37. The video output system according to claim 21 wherein the process of post-processing includes gamma insertion.

10

38. The video output system according to claim 21 wherein the process of post-processing includes color space conversion.

39. The video output system according to claim 21 wherein the process of post-processing includes changing frames of video data into interleaved fields of video data.

15

40. The video output system according to claim 21 wherein the process of post-processing includes addressing on a frame-by-frame basis the video signal being post-processed.

20

41. The video output system according to claim 21 wherein the system is a Peripheral Component Interconnect circuit board.

124975

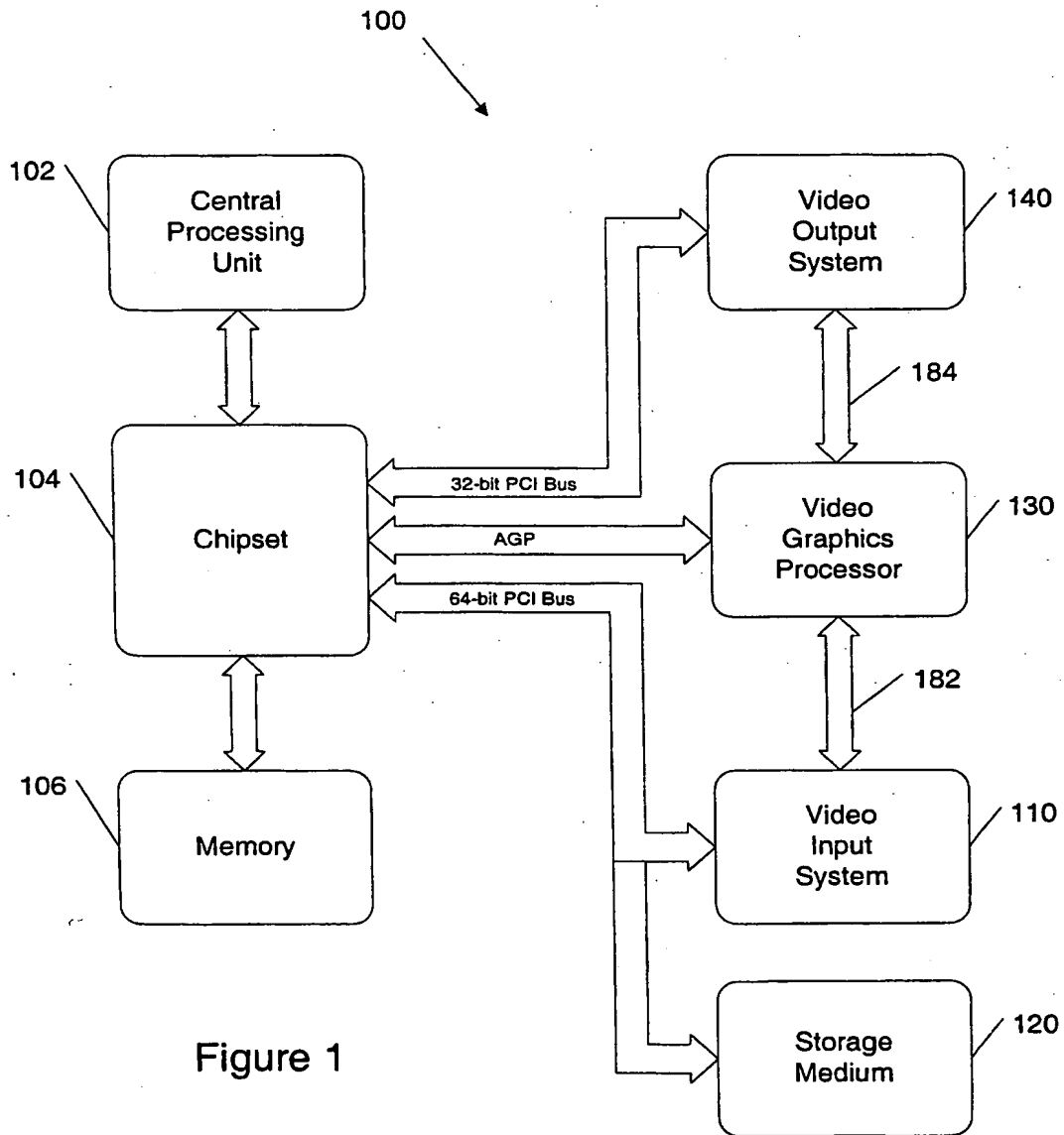


Figure 1

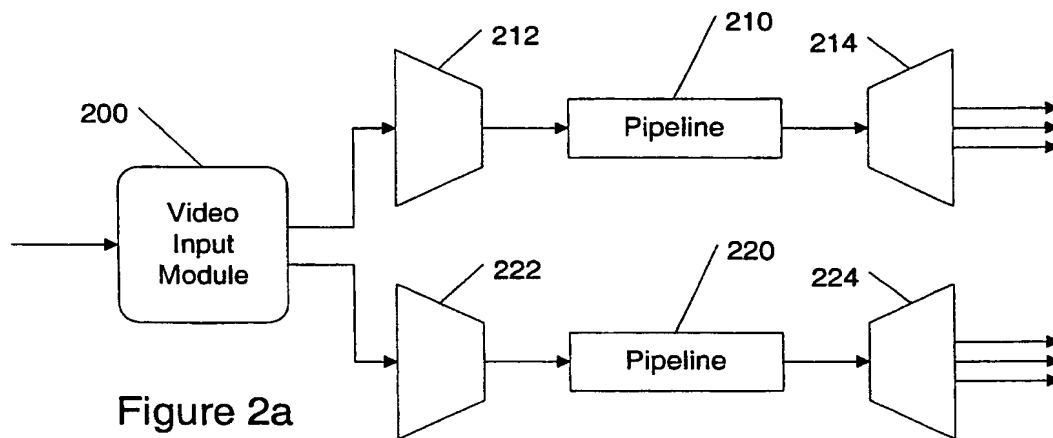


Figure 2a

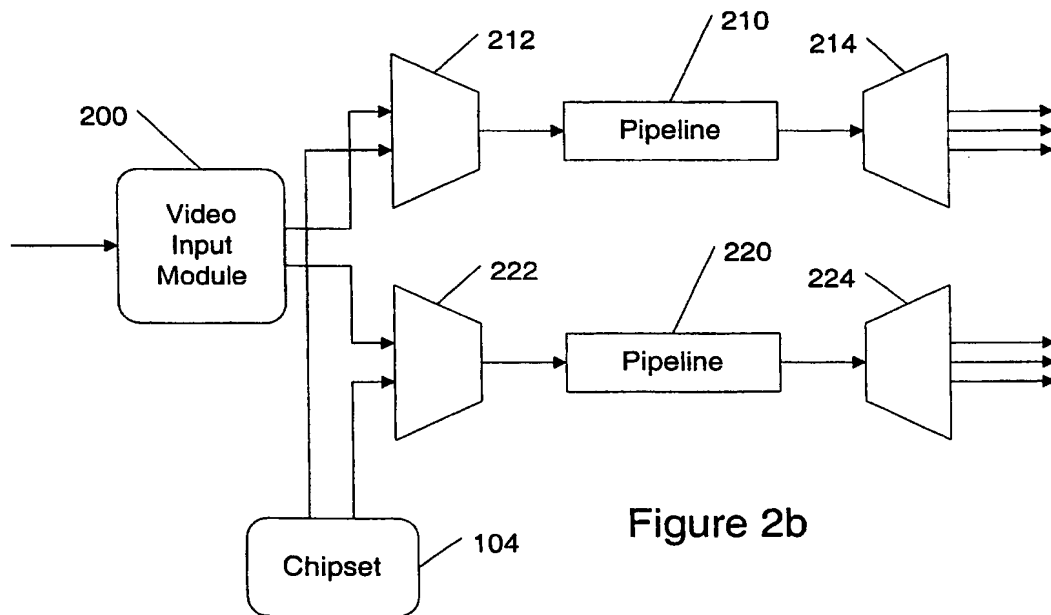


Figure 2b

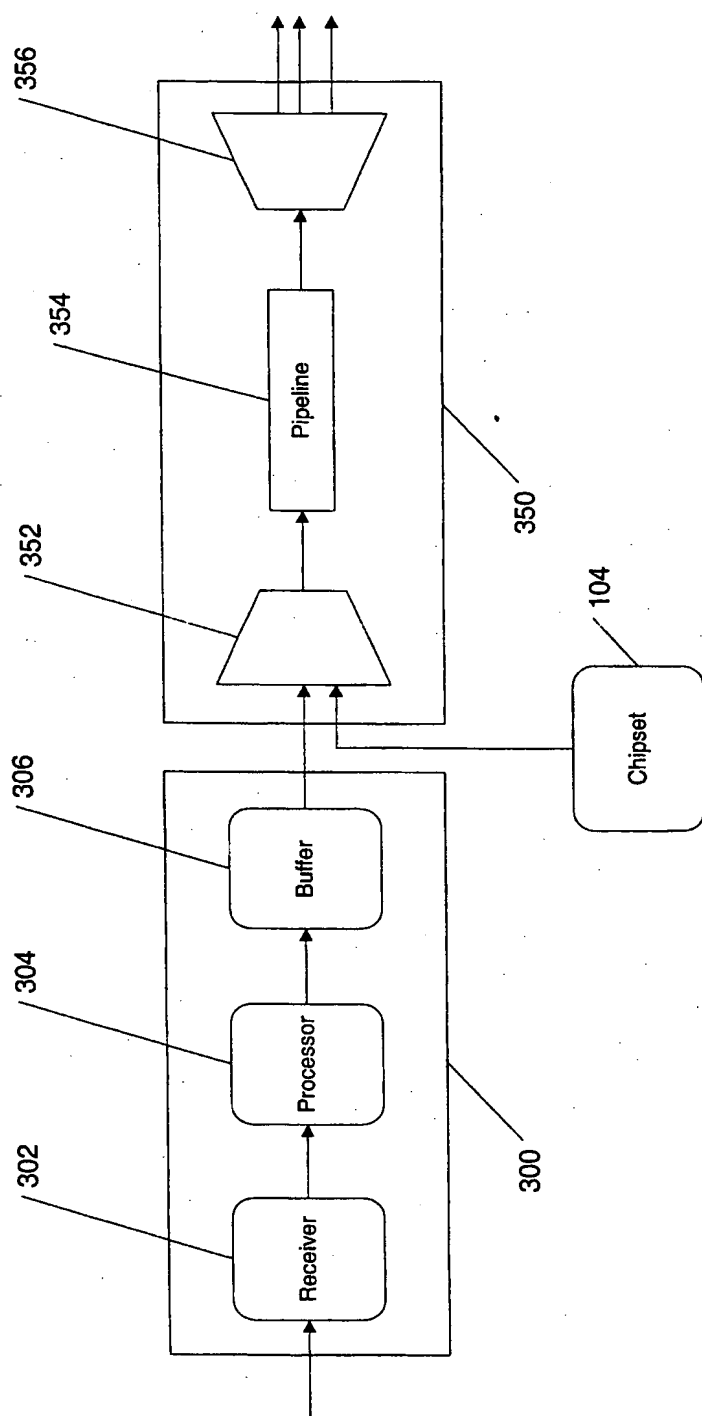
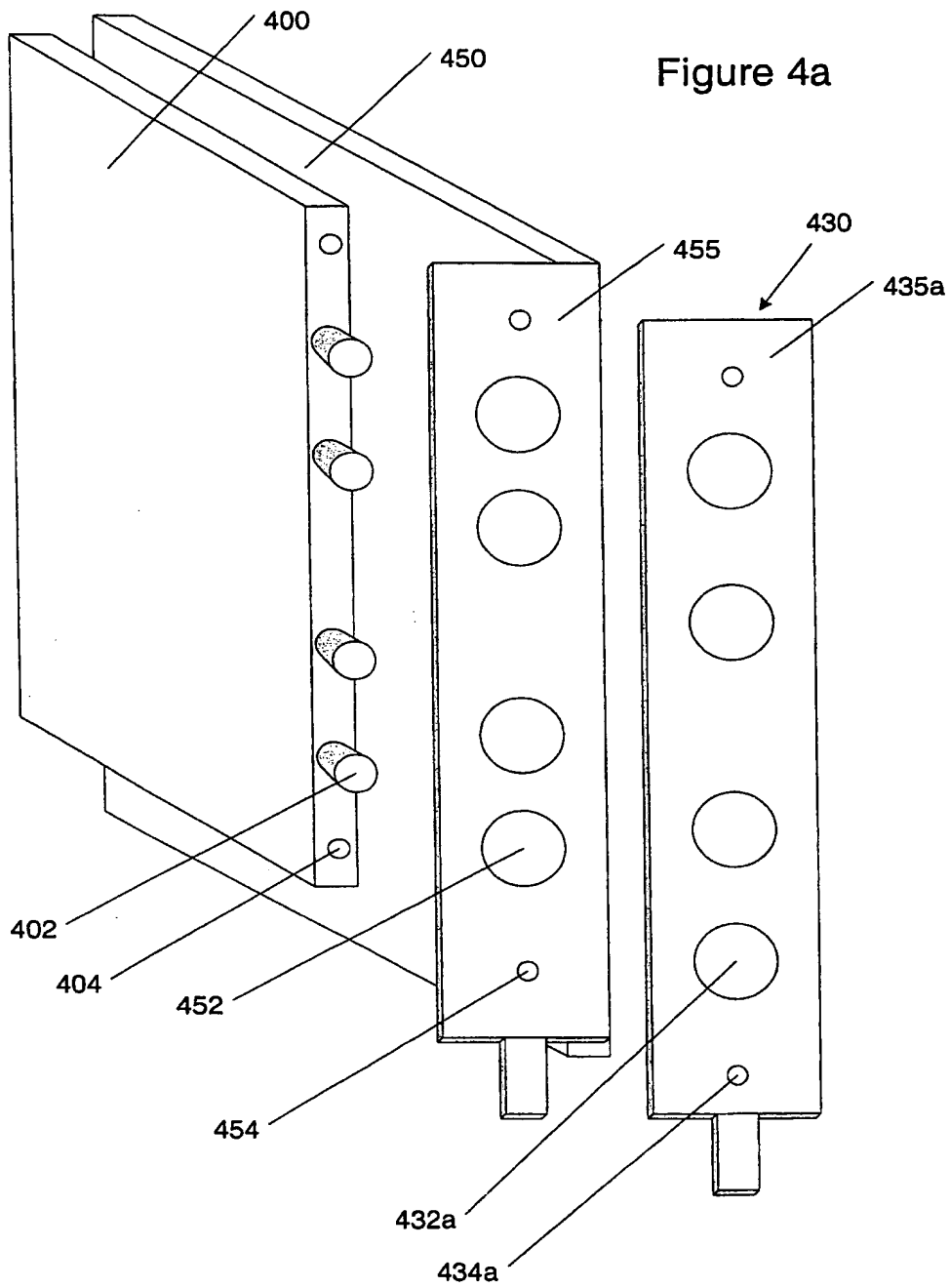
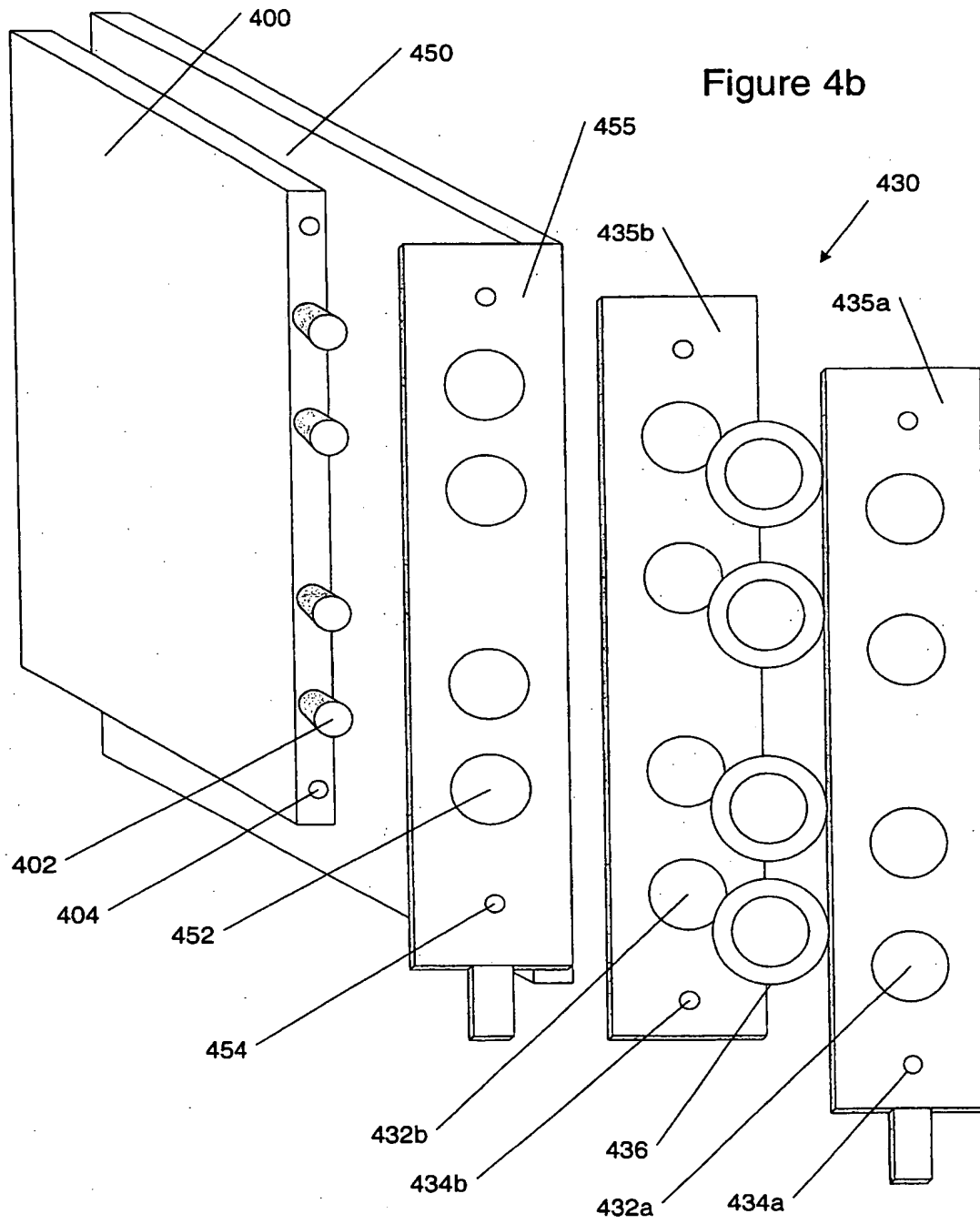


Figure 3





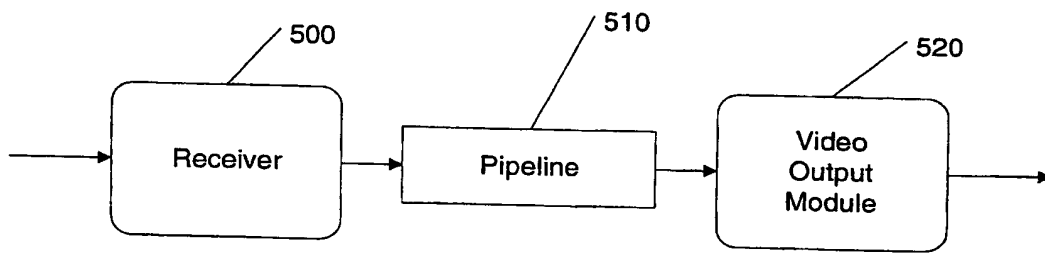


Figure 5

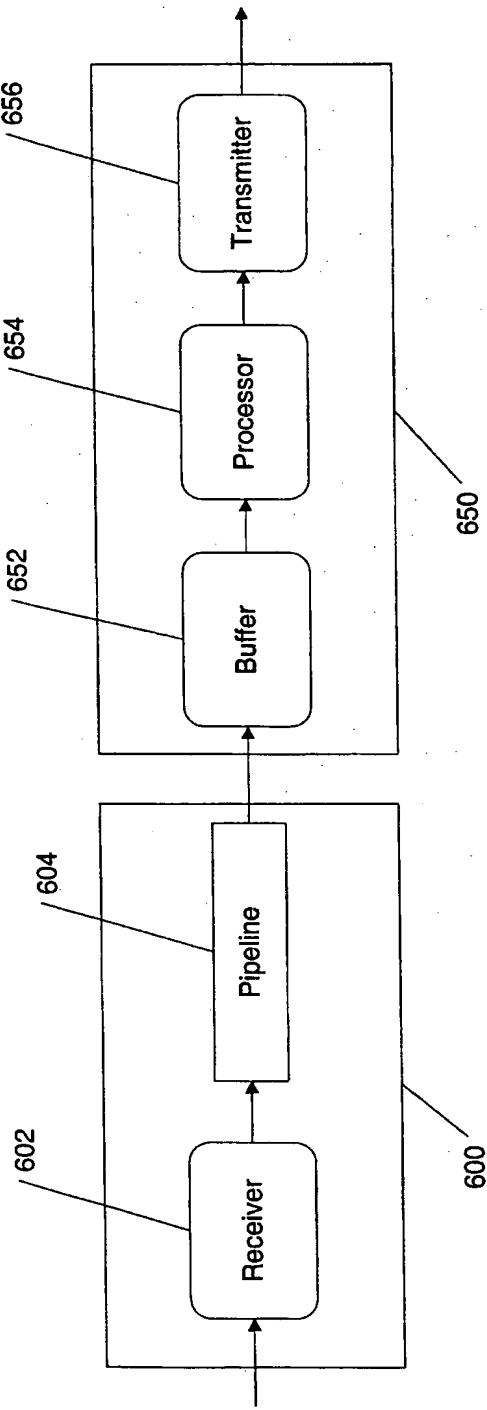


Figure 6

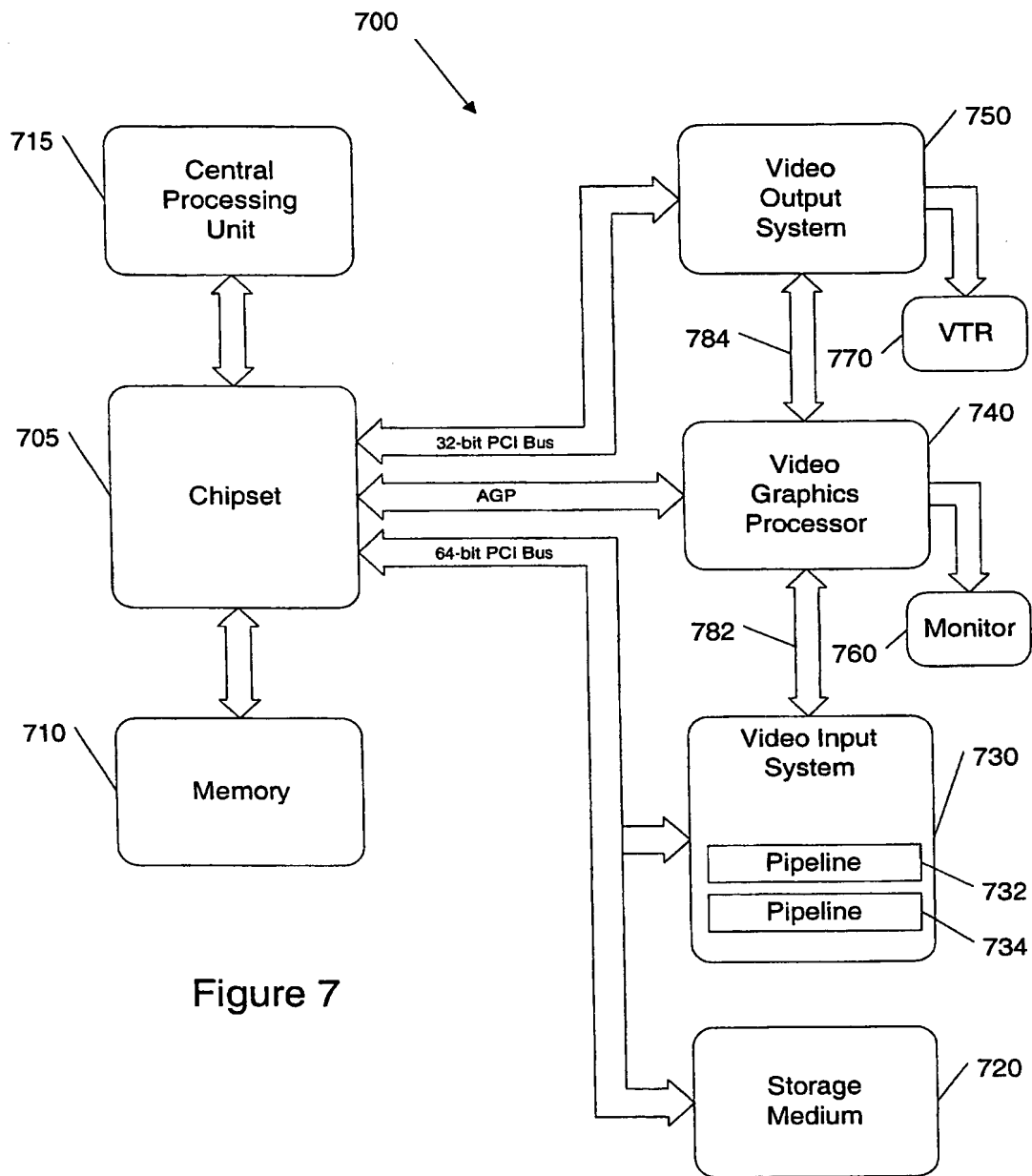


Figure 7

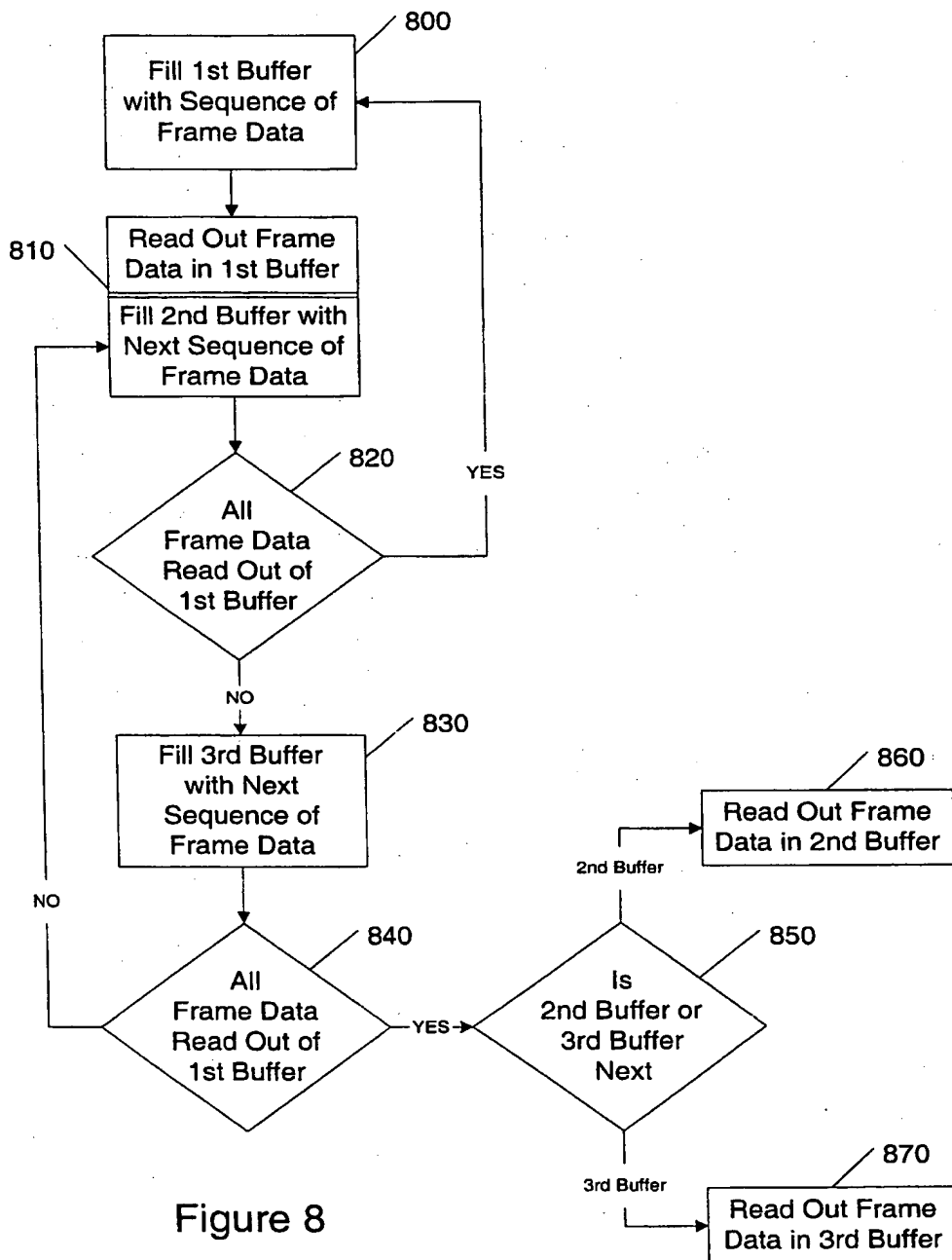


Figure 8

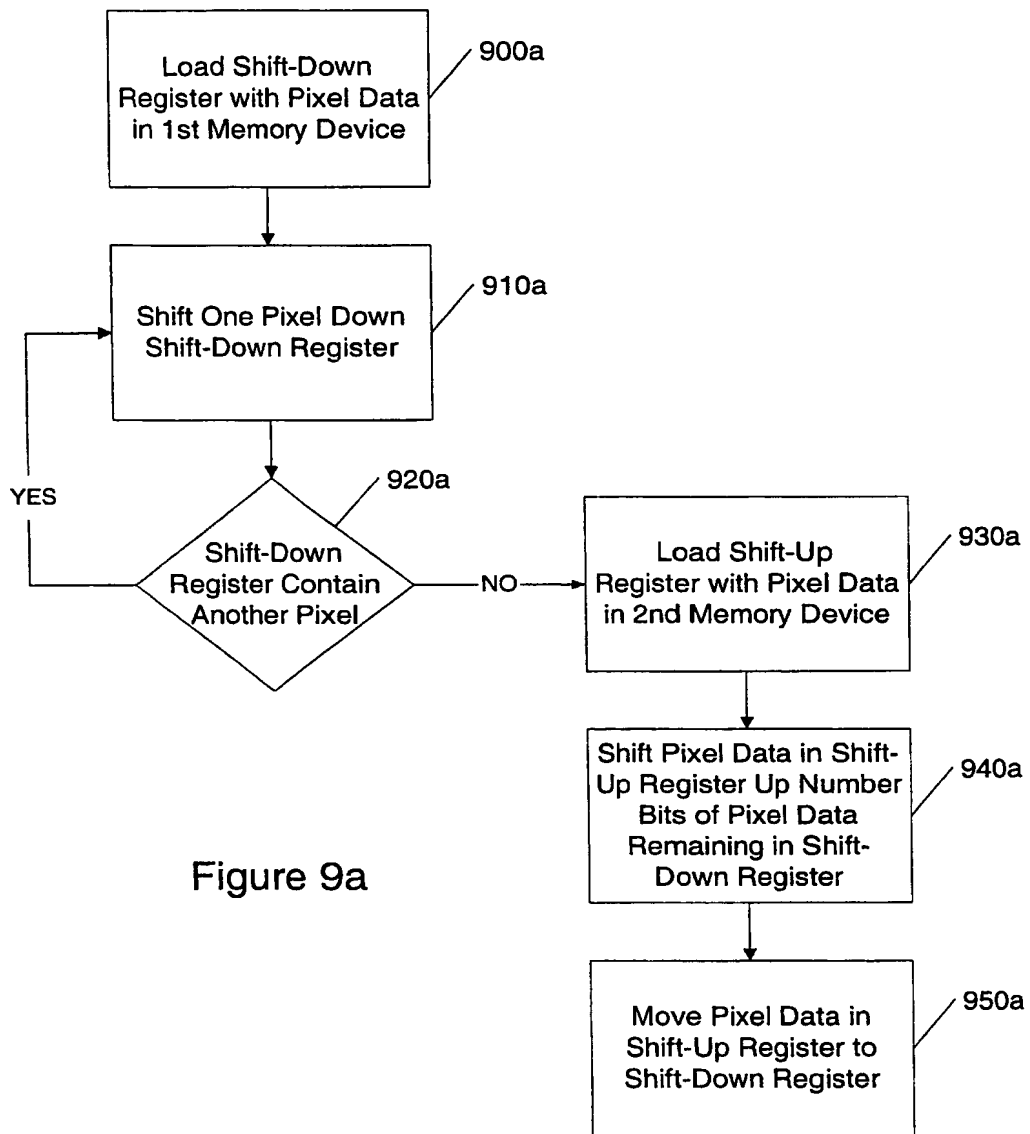


Figure 9a

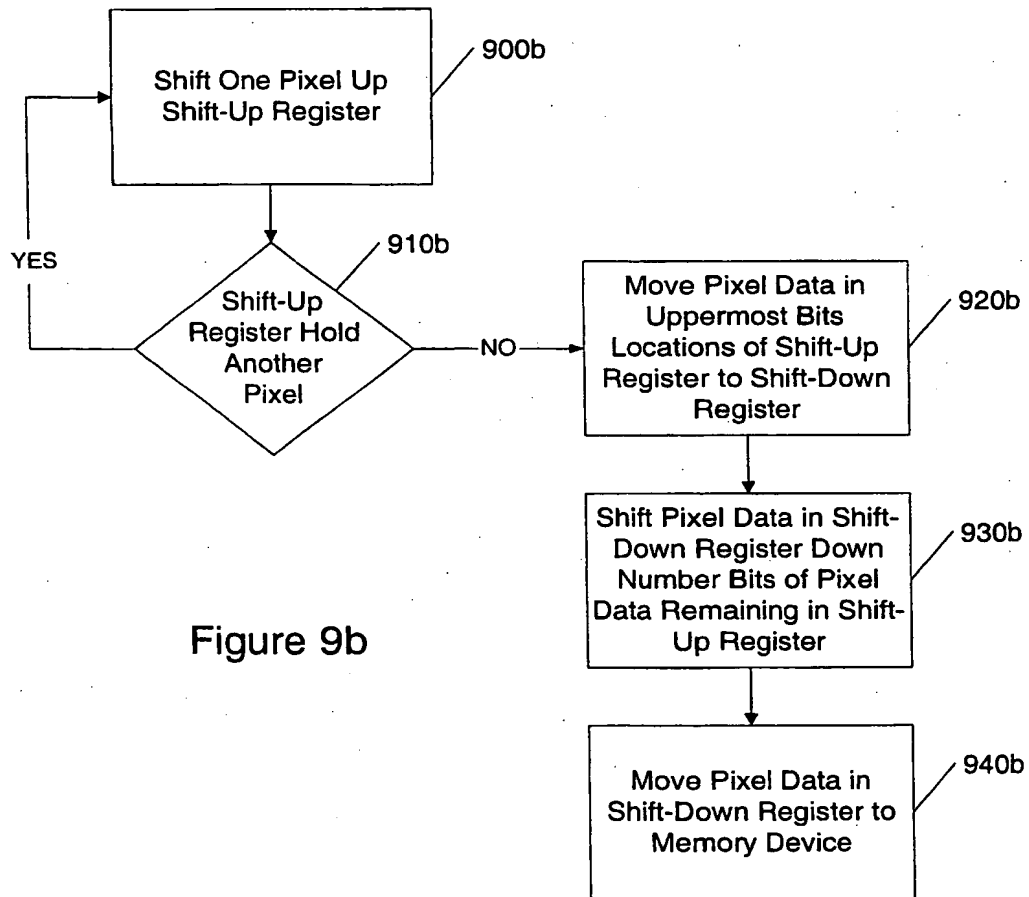


Figure 9b

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 00/21356

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G06F3/14 H04N7/26 G06T1/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G06F H04N G06T

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 93 21574 A (VIDEOLOGIC LTD ;YASSAIE HOSSEIN (GB)) 28 October 1993 (1993-10-28)	1,5,9, 17, 19-21, 24, 26-29, 31,32, 35-41
A	abstract	2,3,7,8, 18,22
	page 3 -page 6 page 9 -page 10	
X	WO 99 12091 A (COLORGRAPHIC COMMUNICATIONS CO) 11 March 1999 (1999-03-11)	1-3,5,8, 9,17,18, 20-22,26
	page 8, line 21 -page 9, line 10	
	--- -/--	

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

* Special categories of cited documents :

- "A" document defining the general state of the art which is not considered to be of particular relevance
- "E" earlier document but published on or after the international filing date
- "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- "O" document referring to an oral disclosure, use, exhibition or other means
- "P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search

9 October 2000

Date of mailing of the international search report

27/10/2000

Name and mailing address of the ISA

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,
Fax: (+31-70) 340-3016

Authorized officer

Marie-Julie, J-M

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 00/21356

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT		
Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 574 748 A (INTEL CORP) 22 December 1993 (1993-12-22) page 3, column 4, line 27 - line 47 page 5, column 8, line 12 - line 26 ---	1,2,5,9, 17,19,20
X	US 5 434 592 A (DINWIDDIE JR JOHN M ET AL) 18 July 1995 (1995-07-18) column 5, line 25 - line 57 ---	1-3,5-7, 9
X	EP 0 867 812 A (TOKYO SHIBAURA ELECTRIC CO) 30 September 1998 (1998-09-30) page 3, column 3, line 15 - line 42 page 4, column 6, line 20 -page 5, column 7, line 21 page 5, column 8, line 46 - line 59 ---	1-3,5-20 21,22
A	WILLNER R: "TRANSFORMING THE PC INTO A TV, RADIO, VCR, AND VIDEO EDITING STUDIO" WESCON TECHNICAL PAPERS,US,WESTERN PERIODICALS CO. NORTH HOLLYWOOD, 7 November 1995 (1995-11-07), pages 743-748, XP000586646 the whole document ---	1,2,4 5-41
X	BACH U ET AL: "MULTIMEDIALES TV-GEREAT" RADIO FERNSEHEN ELEKTRONIK,DE,VEB VERLAG TECHNIK. BERLIN, vol. 45, no. 9, 1 August 1996 (1996-08-01), pages 28,30-31, XP000636538 ISSN: 1436-1574 the whole document ---	1,2,4
X	US 5 929 870 A (TAKEUCHI KESATOSHI) 27 July 1999 (1999-07-27) abstract column 18, line 8 - line 17 ---	1
A	EP 0 493 881 A (IBM) 8 July 1992 (1992-07-08) page 4, column 5, line 17 - line 49 page 4, column 6, line 22 - line 28 ---	1-7,21
A	US 5 799 204 A (PESTO JR WILLIAM STEVE) 25 August 1998 (1998-08-25) column 2, line 56 -column 3, line 8 ---	1,21,22, 26
A	EP 0 814 401 A (TEXAS INSTRUMENTS INC) 29 December 1997 (1997-12-29) the whole document -----	1,21

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/US 00/21356

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 9321574 A	28-10-1993	GB 2271700 A, B US 5977995 A	20-04-1994 02-11-1999
WO 9912091 A	11-03-1999	US 6028643 A AU 9215098 A EP 1010056 A US 6100936 A	22-02-2000 22-03-1999 21-06-2000 08-08-2000
EP 0574748 A	22-12-1993	US 5335321 A DE 69313191 D DE 69313191 T JP 6195468 A US 5640543 A	02-08-1994 25-09-1997 08-01-1998 15-07-1994 17-06-1997
US 5434592 A	18-07-1995	BR 9200321 A CA 2059928 A, C DE 69221341 D DE 69221341 T EP 0498544 A JP 5303358 A	13-10-1992 05-08-1992 11-09-1997 12-02-1998 12-08-1992 16-11-1993
EP 0867812 A	30-09-1998	JP 10116064 A WO 9816887 A	06-05-1998 23-04-1998
US 5929870 A	27-07-1999	US 5680178 A US 5469221 A US 5387945 A WO 9000845 A JP 2298176 A JP 2748562 B JP 2738356 B JP 8095541 A JP 2738286 B JP 7131707 A US 5973706 A US 5986633 A US 5929933 A US 5793439 A	21-10-1997 21-11-1995 07-02-1995 25-01-1990 10-12-1990 06-05-1998 08-04-1998 12-04-1996 08-04-1998 19-05-1995 26-10-1999 16-11-1999 27-07-1999 11-08-1998
EP 0493881 A	08-07-1992	US 5245322 A BR 9105317 A CA 2055054 A, C DE 69113240 D DE 69113240 T JP 4351181 A	14-09-1993 25-08-1992 12-06-1992 26-10-1995 28-03-1996 04-12-1992
US 5799204 A	25-08-1998	NONE	
EP 0814401 A	29-12-1997	US 5841994 A JP 10143651 A	24-11-1998 29-05-1998